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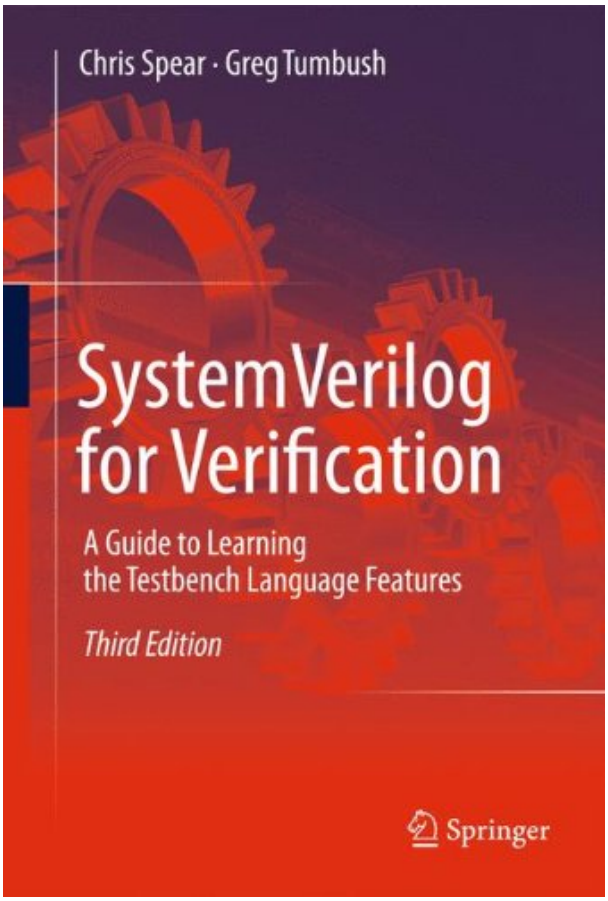

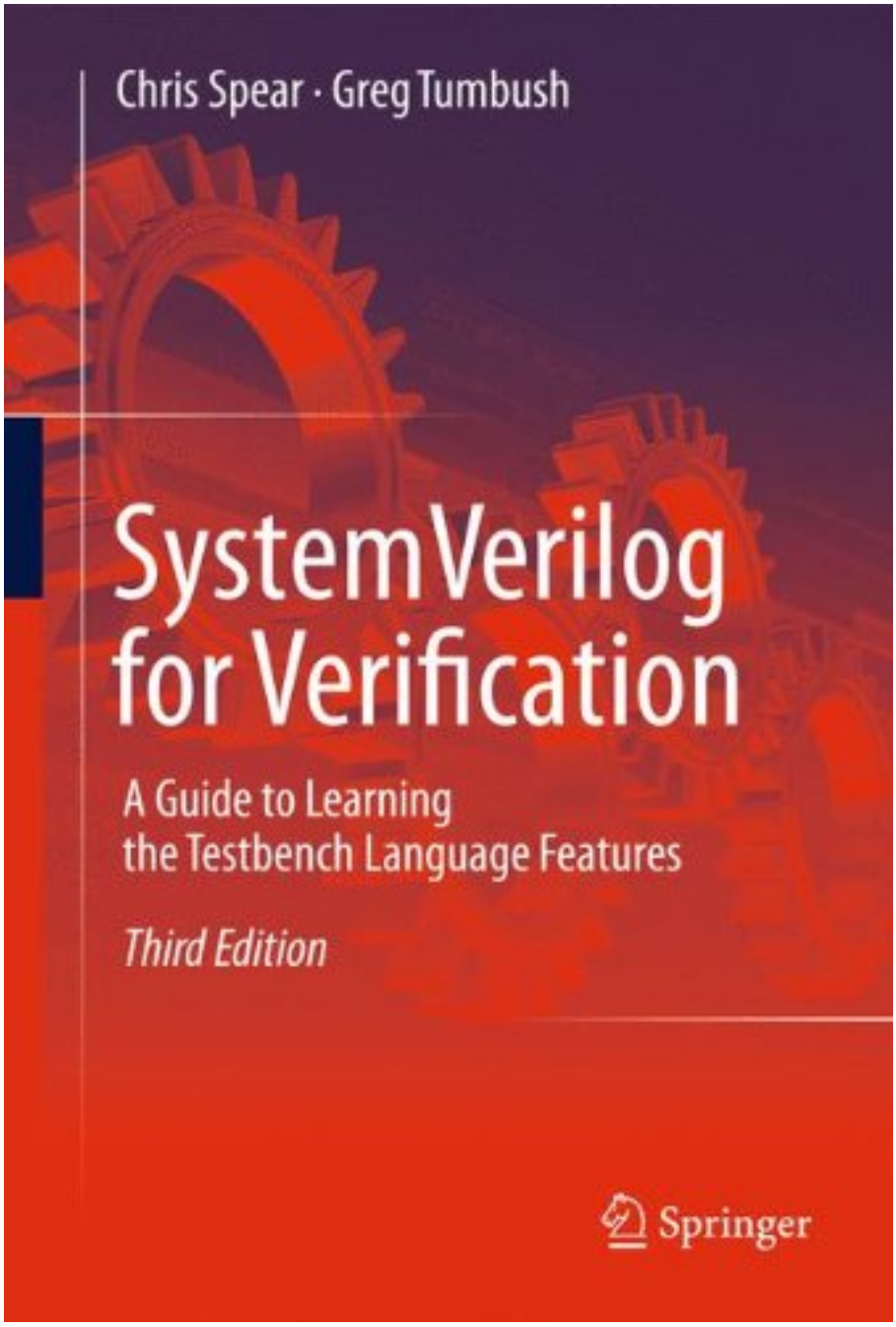

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From the Back Cover

Based on the highly successful second edition, this extended edition of SystemVerilog for Verification: A Guide to Learning the Testbench Language Features teaches all verification features of the SystemVerilog language, providing hundreds of examples to clearly explain the concepts and basic fundamentals. It contains materials for both the full-time verification engineer and the student learning this valuable skill.

In the third edition, authors Chris Spear and Greg Tumbush start with how to verify a design, and then use that context to demonstrate the language features, including the advantages and disadvantages of different styles, allowing readers to choose between alternatives. This textbook contains end-of-chapter exercises designed to enhance students' understanding of the material. Other features of this revision include:

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Features

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Best System Verilog Book I've Seen
By nom_de_plume
Best System Verilog book I own (I have 3 others), I would buy it again. The System Verilog language itself is a bit of a mess, but it is what the industry seems to have settled on. This book presents the language in a coherent and practical manner is quite useful. It provides insights and has saved me a good amount of time.

You won't learn VMM, UVM with this book, you'll learn the basis of the language. If new to System Verilog, or if you never took the time to learn the language in depth then you should read this before you proceed to those. If you've found a good book on VMM or UVM, please post a comment. I've yet to find something to my liking beyond a mechanical treatment.

The book is not perfect. For example section 4.3 (stimulus timing, races) is too loosely explained to be useful when taking what you've learned to practice. Another example: the book barely touches upon packages, and where they can be defined or used. A introductory chapter describing VMM and UVM would also be helpful. So there is room for a fourth edition a few years from now... But this is by far the best System Verilog book I've seen.

5 of 5 people found the following review helpful.
Excellent book except for ...
By Timothy H. Pylant
a few non-compliant code examples that do not follow the IEEE LRM. With that said, overall the book contains a number of good examples and covers the SV language. It doesn't spend much time discussing methodology (which can be good or bad depending on what you're looking for).

In summary, decent reading and a good language reference. Definitely a lot better than the VMM book.

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